Exhibit 1

PATENT
Atty. Dkt. No. 121-0019-US-REG

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Andrew WOLFE	§	
	§	Group Art Unit: 2115
Serial No.: 12/713,220	§	
Confirmation No.: 4243	§	
	§	Examiner: BUTLER, DENNIS
Filed: February 26, 2010	§	
For: PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR	§	

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

RESPONSE TO OFFICE ACTION DATED AUGUST 29, 2012

In response to the non-final Office Action dated August 29, 2012 having a shortened statutory period for response set to expire on November 29, 2012, please enter this response and reconsider the claims pending in the application for the reasons discussed below. Although Applicant believes that no fees are due in connection with this response, the Commissioner is hereby authorized to charge Counsel's Deposit Account No. 50-4588/121-0019-US-REG for any fees, including extension of time fees or excess claims fees, required to make this response timely and acceptable to the Office.

Amendments to the Specification are reflected on page 2 of this paper. **Amendments to the Claims** are reflected in the listing of claims which begins on page 3 of this paper. **Remarks** begin on page 8 of this paper.

IN THE SPECIFICATION:

The following paragraph will replace paragraph [0017] in the as filed application:

[0017] Processing for the transition processing routine [[300]]400 may begin at operation [[302]]402, "receive clock frequency change request." Operation [[302]]402 may be followed by operation [[304]]404, "idle communication between stripes." Operation [[304]]404 may be followed by operation [[306]]406, "examine PLL blocks of requesting stripe and adjacent stripe(s)." Operation [[306]]406 may be followed by operation [[308]]408, "does each of PLL blocks acquire a lock?" Operation [[308]]408 may be followed by either operation [[306]]406 when the decision logic tested at block [[308]]408 fails to be satisfied (NO), or operation [[310]]410, "determine whether to resume communication between stripes", when the decision logic tested at block [[308]]408 is satisfied (YES). Processing for the routine may terminate after block [[310]]410.

IN THE CLAIMS:

The listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A multi-core processor, comprising:

a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input;

a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and

an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.

2. (Original) The multi-core processor of claim 1, the interface block further comprising a first level shifter that is referenced to the second supply voltage and adapted to translate first logic levels associated with the first set of processor cores to second logic levels associated with the second set of processor cores for a first signal traveling from the first set of processor cores to the second set of processor cores.

3. (Original) The multi-core processor of claim 1, the interface block further comprising a second level shifter that is referenced to the first supply voltage and adapted to translate second logic levels associated with the second set of processor cores to first logic levels associated with the first set of processor cores for a second signal traveling from the second set of processor cores to the first set of processor cores.

4. (Original) The multi-core processor of claim 1, wherein the interface block further comprises a synchronizer configured to synchronize the first clock signal and the second clock

signal for communication between one or more processor cores of the first set of processor cores and one or more processor cores of the second set of processor cores.

5. (Original) The multi-core processor of claim 1, wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a periphery of the multi-core processor.

6. (Original) The multi-core processor of claim 1, wherein the first set of processor cores are located in a first region of the multi-core processor, and the second set of processor cores are located in a second region of the multi-core processor.

7. (Original) The multi-core processor of claim 6, wherein the first region and the second region are overlapping regions of the multi-core processor.

8. (Original) The multi-core processor of claim 6, wherein the first region and the second region are non-overlapping regions of the multi-core processor.

9. (Original) The multi-core processor of claim 6, wherein the first region corresponds to a first row of the multi-core processor, and wherein the second region corresponds to a second row of the multi-core processor.

10. (Currently Amended) The multi-core processor of claim 1, wherein the interface block is configured to idle communications between the first set of processor cores and the second set of processor cores when one or more of the first output clock signal and/or the second output clock signal is determined to have changed.

11. (Currently Amended) The multi-core processor of claim 10, wherein the interface block is configured to resume communication between the first set of processor cores and the second set of processor cores after one or more of the first output clock signal and/or the second output clock signal is determined to have stabilized.

12. (Original) The multi-core processor of claim 5, wherein the first set of processor cores is adjacent to the second set of processor cores, and the one or more control blocks are

configured to select the first supply voltage and the second supply voltage to maintain a differential relationship between the first supply voltage and the second supply voltage.

13. (Original) The multi-core processor of claim 12, wherein the differential relationship is based on having an output voltage level associated with the first set of processor cores to be within an acceptable input voltage level associated with the second set of processor cores.

14. (Original) The multi-core processor of claim 1, wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a common region that is substantially central to the first set of processor cores and the second set of processor cores.

15. (Currently Amended) A method for managing communications in a multi-core processor that includes a plurality of processor cores having a first set of processor cores and a second set of processor cores, the method comprising:

idling communications ~~with one or more of the plurality of processor cores~~between the first set of processor cores and the second set of processor cores in response to a clock frequency change request for the first set of processor cores; and

resuming communications ~~with one or more of the plurality of processor cores~~between the first set of processor cores and the second set of processor cores after having determined that a first phase lock loop operation associated with a first clock signal for the first set of processor cores has acquired a first lock signal and a second phase lock loop operation associated with a second clock signal for the second set of processor cores has also acquired a second lock signal, wherein the first clock signal is independent from the second clock signal.

16. (Original) The method of claim 15, wherein resuming communications further comprising having determined that a third phase lock loop operation associated with a third set of processor cores in the multi-core processor has acquired a third lock signal, wherein the third set of processor cores is adjacent to the first set of processor cores.

17. (Original) The method of claim 16, wherein the second set of processor cores is adjacent to the first set of processor cores.

18. (Currently Amended) A non-transistory computer-readable medium containing a sequence of instructions for managing communications in a multi-core processor that includes a plurality of processor cores having a first set of processor cores and a second set of processor cores, which when executed by a computing device, causes the computing device to:

issue a first command to idle communications ~~with one or more of the plurality of processor cores~~between the first set of processor cores and the second set of processor cores in response to a clock frequency change request for the first set of processor cores;

issue a second command to resume communications ~~with one or more of the plurality of processor cores~~between the first set of processor cores and the second set of processor cores after having determined that a first phase lock loop operation associated with a first clock signal for the first set of processor cores has acquired a first lock signal and a second phase lock loop operation associated with a second clock signal for the second set of processor cores has also acquired a second lock signal, wherein the first clock signal is independent from the second clock signal.

19. (Currently Amended) The non-transistory computer-readable medium of claim 18, further including a sequence of instructions, which when executed by the computing device, causes the computing device to determine whether a third phase lock loop operation associated with a third set of processor cores in the multi-core processor has acquired a third lock signal before issuing the second command, wherein the third set of processor cores is adjacent to the first set of processor cores.

20. (Currently Amended) The non-transistory computer-readable medium of claim 19, wherein the second set of processor cores is adjacent to the first set of processor cores.

21. (Currently Amended) A multi-core processor, comprising:

a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage from a power control block and a first output clock signal from a first phase lock loop (PLL) having a first clock signal as input in a clock control block;

a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive

a second supply voltage from the power control block and a second output clock signal from a second PLL having a second clock signal as input in the clock control block, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and

an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.

22. (Currently Amended) The multi-core processor of claim [[1]]21, wherein the interface block is configured to idle communications between the first set of processor cores and the second set of processor cores when one or more of the first output clock signal and/or the second output clock signal is determined to have changed.

23. (Currently Amended) The multi-core processor of claim [[21]]22, wherein the interface block is configured to resume communication between the first set of processor cores and the second set of processor cores after one or more of the first output clock signal and/or the second output clock signal is determined to have stabilized.

REMARKS

This is intended as a full and complete response to the Office Action dated August 29, 2012, having a shortened statutory period for response set to expire on November 29, 2012. By way of this reply, Applicant is amending claims 1, 10-11, 15, and 18-23. Claims 1 – 23 are pending. Applicant is also amending paragraph [0017] in the as filed application, which describes FIG. 4, to correct typographical errors. No new matter has been added.

Examiner Interview

Applicant thanks Examiner Butler for the November 27, 2012 telephone interview. The interview included discussions of the 35 U.S.C. § 101 rejections, 35 U.S.C. § 112 rejections, 35 U.S.C. § 102, and 35 U.S.C. § 103 rejections in view of the references cited in the Office Action. An agreement was reached regarding the 35 U.S.C. § 101 rejections and the 35 U.S.C. § 112 rejections. Pending the Examiner's further searches, the Examiner acknowledges that the architecture shown and described in the present disclosure differs from the currently cited references.

Applicant respectfully submits that the claims as presented in this response substantially reflect the discussions during the interview.

Claim Objections

Claims 22 – 23 are objected to under 37 CFR 1.75 as allegedly being substantial duplicates of claims 10 and 11. Claims 22 – 23 have been amended to depend on claims 21 and 22, respectively. Claim 21 also recites different elements than claim 1 (e.g., a power control block and a clock control block). Applicant respectfully requests the withdrawal of the claim objections.

35 U.S.C. § 101 Rejection

Claims 18 – 20 are rejected under 35 U.S.C. §101, because the claimed invention is allegedly directed to non-statutory subject matter. The suggested "non-transitory" language has been added, and Applicant respectfully requests the withdrawal of the rejections under 35 U.S.C. §101.

35 U.S.C. § 112 Rejection

Claims 15 – 20 are rejected under 35 U.S.C. §112, second paragraph for being allegedly indefinite and failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. As discussed during the interview, Applicant has amended

independent claims 15 and 18 to clarify that the communication is "between the first set of processor cores and the second set of processor cores." The amendments are at least supported by paragraph [0018] and FIG. 1, FIG. 3, and FIG. 4 of the as filed application. Applicant respectfully requests the withdrawal of the rejections under 35 U.S.C. §112.

35 U.S.C. § 102 Rejections

Claims 1, 5 – 6, 8 – 9, 14 and 21 are rejected under 35 U.S.C. §102(e) as being allegedly anticipated by U.S. Patent Application Publication 2009/0106576 (hereinafter *Jacobowitz*).

Applicant does not concede that the above reference is prior art and reserves the right to challenge the reference at a later date. Further, Applicant respectfully submits that the rejections are overcome for at least the reasons stated below.

To anticipate a claim, the alleged reference must teach each and every element of the claim. Applicant respectfully submits that *Jacobowitz* does not teach or suggest one or more elements of the amended independent claims 1 and 21. Specifically, *Jacobowitz* does not teach or suggest at least the elements of "a first set of processor cores… configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (LLP) having a first clock signal as input," "a second set of processor cores… configured to dynamically received a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal." The claim amendments are at least supported by paragraph [0015] and FIG. 3 of the as filed application.

First, *Jacobowitz* fails to disclose or teach a first set of processor cores and second set of processor cores configured to dynamically receive a first supply voltage and a second supply voltage, respectively. In addition, the first supply voltage is <u>independent from</u> the second supply voltage, as required in the amended independent claims 1 and 21. Paragraph [0043] of *Jacobowitz* merely mentions that "[f]urther power management can be realized by controlling the power supply voltage (Vdd) to each core and/or chip." In other words, *Jacobowitz* is silent with respect to least the recited different <u>sets of processor cores</u> configured to receive <u>independent</u> supply voltages.

Second, FIG. 6 and all other figures of *Jacobowitz* clearly show that the microprocessor chip (e.g., 600) receives a system reference oscillator clock frequency (v_R) and distributes v_R to local oscillators 108. <u>See</u> *Jacobowitz*, paragraphs [0037]-[0038] and FIG. 6. *Jacobowitz* fails to

disclose or teach a first set of processor cores and second set of processor cores configured to dynamically receive a first output clock signal of a first PLL having a first clock signal as input and a second output clock signal of a second PLL having a second clock signal as input, respectively. In addition, the first clock signal is independent from the second clock signal, as required in the amended independent claims 1 and 21.

For at least the reasons set forth above, the amended independent claims 1 and 21 and the related dependent claims 2 – 14 and 22 – 23 are patentable over *Jacobowitz*. Applicant respectfully requests the withdrawal of the rejections under 35 U.S.C. §102.

35 U.S.C. § 103 Rejections

Claims 2 – 4, 7, 12 and 13 are rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over *Jacobowitz* in view of U.S. Patent Application Publication 2009/0138737 (hereinafter *Kim*).

Claims 10 – 11, 15 – 20 and 22 – 23 rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over *Jacobowitz* in view of Kim and further in view of U.S. Patent Application Publication 2010/0188115 (hereinafter *von Kaenel*).

Applicant does not concede that the aforementioned references are prior art and reserves the right to challenge these references at a later date. Further Applicant respectfully submits that these rejections are overcome for at least the reasons stated below.

To establish a *prima facie* case of obviousness required for a §103(a) rejection, the references must teach or suggest all the claim elements.

Claims 2 – 4, 7, 12 and 13

As discussed during the interview, *Kim* discloses a different architecture than the one recited in the present disclosure. Specifically, as shown in FIG. 1 and FIG. 2 of *Kim*, *Kim* fails to disclose or teach a first set of processor cores and second set of processor cores configured to dynamically receive a first supply voltage and a second supply voltage, which is independent from the first supply voltage, respectively. Instead, *Kim* discloses having each core, not a set of processor cores, received a V_{DD} (i.e., V_{DD1}, V_{DD2}, V_{DD3}, and V_{DD4}).

In addition, *Kim* also fails to disclose or teach a first set of processor cores and second set of processor cores configured to dynamically receive a first output clock signal of a first PLL having a first clock signal as input and a second output clock signal of a second PLL having a second clock signal, respectively. In addition, the first clock signal is independent from the second clock signal. Instead, *Kim* discloses the apparatus comprising a multi-core processor (i.e., 100 in FIG. 1 or 200 in FIG. 2) having a single clock source (i.e., 170 in FIG. 1 or 270 in

FIG. 2). The clock signal from this single clock source is then processed (i.e., divided or multiplied) and provided to each of the cores. See *Kim*, paragraphs [0024]-[0025] and FIGs 1 – 2.

Moreover, the Examiner acknowledges that *Jacobowitz* does not disclose the recited first and second level shifters in claims 2 and 3. See Office Action, page 7. *Kim* merely discloses a voltage level-translating communication transceiver 180 that is "configured to enable communications between each of the plurality of cores 110, 120, 130, and 140." See *Kim*, paragraph [0024]. *Kim* is silent with respect to the recited "first level shifter that is referenced to the second supply voltage" (which is independent from the first supply voltage) and "adapted to translate… for a first signal traveling from the first set of processor cores to the second set of processor cores" in claim 2. *Kim* is also silent with respect to the recited "second level shifter that is referenced to the first supply voltage" and "adapted to translate… for a second signal traveling from the second set of processor cores to the first set of processor cores."

For at least the reasons set forth above, *Kim* fails to cure the deficiencies of *Jacobowitz*.

Claims 10 – 11, 15, 18 and 22 – 23

The Examiner acknowledges neither *Jacobowitz* nor *Kim* discloses the recited operations of idling communications and resuming communications. See Office Action, page 8. Applicant respectfully submits that none of *Jacobowitz*, *Kim*, and *von Kaenel* discloses or teaches at least "resuming communications… after having determined that a first phase lock loop operation associated with a first clock signal for the first set of processor cores has acquired a first lock signal and a second phase lock loop operation associated with a second clock signal for the second set of processor cores has also acquired a second lock signal, wherein the first clock signal is independent from the second clock signal," as required in the amended independent claims 15 and 18.

As discussed above, neither *Jacobowitz* nor *Kim* discloses having sets of processor cores configured to receive multiple and independent clock signals. In conjunction with its FIG. 9, *von Kaenel* merely describes "wait[ing] for the clock generation circuit to lock to the new frequency (block 148)" in paragraph [0074]. *von Kaenel* is silent with respect to at least the recited elements of "idling communication… in response to a clock frequency change request" and "resuming communication" after having determined the acquisition of PLL lock signals associated with multiple independent clock signals.

For at least the reasons set forth above, *von Kaenel* fails to cure the deficiencies of *Jacobowitz* and *Kim*.

Thus, claims 2 – 4, 7, 10 – 13, 15 – 20, and 22 - 23 are patentable over *Jacobowitz*, *Kim*, and *von Kaenel*. Applicant respectfully requests the withdrawal of the rejections under 35 U.S.C. §103.

CONCLUSION

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that the claims be allowed. If there are any questions about any of the foregoing, please contact Applicant's undersigned representative.

Respectfully submitted,

/Gene Su/

Gene Su
Attorney for Applicant(s)
Registration No. 45,140

Telephone: (886) 2.2700.7882
Facsimile 1: (886) 2.2700.7856
Facsimile 2: (650) 644.3217
Email: filing@suipconsulting.com